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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit : 2815

Applicants : Kazuo AOYAMA, et al.

Serial No. : 09/754,632

Filed : January 4, 2001

For : FUNCTION RECONFIGURABLE SEMICONDUCTOR DEVICE AND INTEGRATED CIRCUIT CONFIGURING THE SEMICONDUCTOR DEVICE

Assistant Commissioner for
Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.56

S I R :

Applicants wish to bring to the attention of the Examiner the following publications:

1. Hiroshi Sawada, Kazuo Aoyama, Akira Nagoya and Kazuo Nakajima, "Consideration for a Reconfigurable Logic Device using Neuron MOS Transistor", TECHNICAL REPORT OF IEICE. CPSY99-89, pp. 41-48, November 27, 1999.

2. Kazuo Aoyama, Hiroshi Sawada, Akira Nagoya and Kazuo Nakajima, "A Design Method for a Circuit with Neuron MOS Transistors Realizing any Symmetric Function", TECHNICAL REPORT OF IEICE. CPSY99-90, pp. 49-56, November 27, 1999.

3. Kazuo Aoyama, Hiroshi Sawada, and Akira Nagoya "A Method for Designing a Circuit with Neuron MOS Transistors Realizing any Logic Function", The 13th Workshop on Circuits and Systems in Karuizawa, pp. 113-118, April 24-25, 2000.

4. Kazuo Aoyama, Hiroshi Sawada, and Akira Nagoya "A Design of a Circuit with Neuron MOS Transistors Realizing any Symmetric Function", PROCEEDINGS OF THE 2000 IEICE GENERAL CONFERENCE, p. 85, March 31, 2000.

5. Japanese laid-open patent application No. 7-161942.

6. Japanese laid-open patent application No. 6-77427.

7. Kazuo Aoyama, Hiroshi Sawada, Akira Nagoya, and Kazuo Nakajima, "A Threshold Logic-Based Reconfigurable Logic Element with a New Programming Technology", 10th International Conference, FPL 2000, pp. 665-674, August 30, 2000.

8. Tadashi Shibata, and Tadahiro Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 39, No. 6, pp. 1444-1455, June, 1992.

9. Tadashi Shibata, Koji Kotani, Tadahiro Ohmi, "Real-Time Reconfigurable Logic Circuits Using Neuron MOS Transistors," International Solid-State Circuits Conference, 1993.

10. S.D. Brown, et al. "Field-Programmable Gate Arrays," Kluwer Academic Publishers.

These publications are listed on the attached form PTO-1449 and copies are enclosed for the convenience of the Examiner, along with English translations of the foreign publications.

It is requested that these publications be considered and made of record herein.

The Office is hereby authorized to charge Deposit Account No. 11-0600 for any fees required by this paper, a copy of which is enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on

Date April 3, 2001 Atty's Reg. # 18,918

Atty's Signature Edward W Greason

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EDWARD W. GREASON

Respectfully submitted,

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Dated: April 3, 2001

Form PTO-1449 (REV. 2-32) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
	09/754,632
APPLICANT: Kazuo AOYAMA, et al	
FILING DATE: Jan. 4, 2001	GROUP: 2815

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		7-1 619 42	6/23/95	Japan			X	
		6-7 742 7	3/18/94	"			X	

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Hiroshi Sawada, et al., "Consideration for a Reconfigurable Logic Device using Neuron MOS Transistor", TECHNICAL REPORT OF IEICE. CPSY99-89, pp. 41-48, Nov. 27, 1999
		Kazuo Aoyama,et al., "A Design Method for a Circuit with Neuron MOS Function", TECHNICAL REPORT OF IEICE. CPSY99-90, pp. 49-56, Nov. 27, 1999.
		Kazuo Aoyama, et al., "A Method for Designing a Circuit wit Neuron MOS Transistors Realizing any Logic Function", The 13th Workshop on Circuits and Systems in Karuizawa, pp. 113-118, April 24-25, 2000.

EXAMINER: _____ DATE CONSIDERED: _____

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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✓	✓	Kazuo Aoyama, et al., "A Design of a Circuit with Neuron MOS Transistors Realizing Any Symmetric Function", proceedings of the 2000 IEICE GENERAL CONFERENCE, pp. 855 March 31, 2000.
		~~Kazuo Aoyama, et al., "A Threshold Logic-Based Reconfigur~~able Logic Element with a New Programming Technology", ~~10th International Conference, FPL 2000, pp. 665-674,~~ August 2000

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Form PTO-1449 (REV. 2-93) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

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		Tadashi Shibata, et al., "A Functional MDS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 39, No. 6, pp. 1444-1455, June 1992.
		~~Tadashi Shibata, et al., "Real Time Reconfigurable Logic~~ Circuits Using Neuron MOS Transistors", International Solid-State Circuits Conference, 1993.
	✓	S.D. Brown, et al., "Field-Programmable Gate Arrays", Kluwer Academic Publishers

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